

that is negatively doped, i.e., doped with a negative charge. A p-type top layer 120 of the LDMOS device 100 is formed on top of the n-type region 105 and serves as a RESURF region. As mentioned, the p-type buried layer 115 and the p-type top layer 120 function as RESURF regions, which means they serve to reduce an electric field in their respective adjacent n-type regions 105.

A drain electrode 125 is coupled to a highly negatively doped (n+) implant 130 that is embedded in the n-type region 105. The drain electrode 125 serves as the drain of the n-type LDMOS transistor of the integrated circuit 100. The drain electrode 125 of the n-type transistor is also electrically coupled to a second electrical contact 135 that is coupled to a highly positively doped (p+) implant 140, or region, that is embedded in the n-type region 105. The second contact 135 serves as the source of the PMOS transistor that is embedded in the integrated circuit 100. The source of the PMOS transistor will at times be referred to herein as the p-source 135.

A source electrode 145 is coupled to a highly negatively doped (n+) implant 150 that is embedded in a p-type well 165 within the n-type region 105. The source electrode 145 serves as the source of the n-type LDMOS transistor of the integrated circuit 100. The source electrode 145 of the n-type transistor is also electrically coupled to a second electrical contact 170 that is coupled to a highly positively doped (p+) implant 175 that is embedded in the top p-type layer 120. The second contact 170 forms the drain of the PMOS transistor that is embedded in the integrated circuit 100. The p-type top RESURF region 120 thus serves as a drain extension of the PMOS. Said second contact 170 constituting the drain of the p-type transistor will at times be referred to herein as the p-drain. In an illustrative embodiment, the source electrode 145 of the n-type transistor is also electrically coupled to a third electrical contact 155 that is coupled to a highly positively doped (p+) implant 160 that is embedded in the p-well 165. The third contact 155 forms part of the drain of the PMOS transistor, together with the drain contact 170 coupled to the top p-type layer 120. In such an embodiment, the buried p-type RESURF region 115 thus serves as a further drain extension of the PMOS.

The voltage present at the n-gate 180 controls the current flow from the drain 125 to the source 145 of the n-type LDMOS transistor of the integrated circuit 100. The drain-to-source current I_{ds-n} of the n-type transistor comprises electrons flowing from the source 145 to the drain 125 in the top and bottom channels of the n-type region 105, as shown in FIG. 1.

The voltage present at the p-gate 185 controls the current flow from the source 135 of the p-type transistor to the drain 170 of the p-type transistor of the integrated circuit 100. In an illustrative embodiment, the source-to-drain current I_{sd-p} of the p-type transistor comprises holes flowing from the p-source 135 to the p-drain 170 in the top p-type layer 120, as shown in FIG. 1. This flow of electrons in one channel (the n-region 105) and the flow of holes in the opposite direction in another channel (the top p-type layer 120) is referred to herein as p-n bimodal conduction. It is important to note that the bimodal conduction is still unipolar conduction, with the electron and hole flows confined in separate conduction paths.

In an illustrative embodiment, the source-to-drain current I_{sd-p} further comprises holes flowing from the p-source 135 to the p-drain 155 in the buried p-type layer 115. In an illustrative embodiment, the integrated circuit 100 includes, at spaced intervals in the device width direction (i.e., the 3rd dimension of FIG. 1) of the LDMOS device 100, positively

doped regions (not shown in FIG. 1) connecting the buried p-type layer 115 to the p-well 165, in order to facilitate current flow between the p-drain 155 and the buried p-type layer 115. For example, in one embodiment such p-type regions are placed at intervals of approximately every 20 μm in the width direction of the LDMOS device 100. Placing these p-type regions at spaced intervals as opposed to having a continuous connection between the buried p-type layer 115 and the p-well 165 allows current (in the form of holes) to flow between the p-drain 155 and the buried p-type layer 115 while still allowing current (in the form of electrons) to flow in the n-type region 105 between the source 145 and the bottom channel. Similarly, in an illustrative embodiment, the integrated circuit 100 also includes, at spaced intervals in the width direction, positively doped regions (not shown in FIG. 1) connecting the buried p-type layer 115 to the top p-type layer 120 proximate the p-source 135, in order to facilitate current flow between the p-source 135 and the buried p-type layer 115. Placing these p-type regions at spaced intervals as opposed to having a continuous connection between the buried p-type layer 115 and the top p-type layer 120 allows current (in the form of holes) to flow between the p-source 135 and the buried p-type layer 115 while still allowing current (in the form of electrons) to flow in the n-type region 105 between the drain 125 and the top channel. These vertical diffusion connections must be carefully designed to avoid localized premature breakdown in the OFF state.

The high voltage p-n bimodal LDMOS integrated circuit 100 can block voltage only when both the n-channel 105 and p-channel 120 are turned off. The device 100 can be used as an NMOS transistor when the n-channel is on (conducting), as a PMOS transistor when the p-channel is on, or as a synchronized switch when both channels are on simultaneously. When both the n-channel and p-channel are conducting simultaneously, the total drain-to-source current flow I_{ds-pn} of the bimodal LDMOS device 100 is equal to the sum of the net drain-to-source current I_{ds-n} of the n-type LDMOS plus the net source-to-drain current I_{sd-p} of the slave PMOS. Thus the total drain-to-source current I_{ds-pn} of the bimodal LDMOS integrated circuit 100 is enhanced, both in the linear region of the I_{ds} curve and in the saturation region. With electron flow in the n-drift region 105 and hole flow in the p-type (RESURF) region 120, p-n conduction in parallel reduces the specific on-resistance R_{sp} and improves drive current. In the illustrative embodiment wherein the buried p-type RESURF layer 115 is used as a further drain extension of the slave PMOS by periodically forming vertical p-type connections in the device width direction, bimodal p-n conduction is further enhanced.

FIG. 2 is a schematic circuit diagram of a dual-gate p-n bimodal conduction LDMOS transistor. The dual-gate LDMOS transistor 100 of FIG. 2 illustratively corresponds to the LDMOS integrated circuit of FIG. 1. Thus elements common to FIGS. 1 and 2 are identified with like reference numbers. The LDMOS dual-gate p-n transistor 100 of FIG. 2 comprises an NMOS transistor 200 and a PMOS transistor 210. NMOS transistor 200 comprises a drain terminal 125, source terminal 145, and a gate terminal 180. The voltage present at the gate terminal 180 dictates in part the flow of current from the drain 125 to the source 145, as is described above with respect to FIG. 1. PMOS transistor 210 comprises a source terminal 135, drain terminal 170, and a gate terminal 185. The voltage present at the gate terminal 185 dictates in part the flow of current from the source 135 to the drain 170, as is described above with respect to FIG. 1. The drain 125 of the NMOS transistor 200 is coupled to the source 135 of the PMOS transistor 210, and the source 145